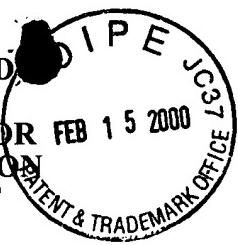


FORM PTO-1449 (MODIFIED)



LIST OF PUBLICATIONS FOR  
APPLICANT'S INFORMATION  
DISCLOSURE STATEMENT

Applicant:  
Case:  
Serial No.:  
Filing Date:  
Group:

K. Azadet, E.F. Haratsch  
10-2  
09/471,920  
December 23, 1999  
2739 2631

#3

U.S. PATENT DOCUMENTS

EXAMINER	INITIAL	DOCUMENT NO.	DATE	NAME	FILING DATE	CLASS/SUBCLASS	IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

EXAMINER	INITIAL	DOCUMENT NO.	DATE	COUNTRY	TRANSLATION	CLASS/SUBCLASS	YES	NO

OTHER DOCUMENTS

EXAMINER	INITIAL	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.

- |    |   |
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| 1. | Fettweis et al., "High-Speed Parallel Viterbi Decoding: Algorithm and VLSI-Architecture," IEEE Communications Magazine, May 1991.   |
| 2. | Chevillat et al., "Decoding of Trellis-Encoded Signals in the Presence of Intersymbol Interference and Noise," IEEE Transactions on Communications, Vol. 37, No. 7, July 1989.                                      |
| 3. | Erich F. Haratsch, "High-Speed VLSI Implementation of Reduced Complexity Sequence Estimation Algorithms with Application to Gigabit Ethernet 1000Base-T," Bell Laboratories, Lucent Technologies, Holmdel, NJ, USA. |
| 4. | K. Azadet, "Gigabit Ethernet over Unshielded Twisted Pair Cables," Bell Laboratories, Lucent Technologies, Holmdel, NJ, USA.  |
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Phuong Phan

21/11/03

Examiner

Date Considered

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.

## FORM PTO-1449 (MODIFIED)

LIST OF PUBLICATIONS FOR  
APPLICANT'S INFORMATION  
DISCLOSURE STATEMENT

#5

Applicant: Azadet, E.F. Haratsch  
 Case: 10-2  
 Serial No.: 09/471,920  
 Filing Date: December 23, 1999  
 Group: 2739 2631



## U.S. PATENT DOCUMENTS

EXAMINER	INITIAL	DOCUMENT NO.	DATE	NAME	CLASS/SUBCLASS	FILING DATE	IF APPROPRIATE
	HH	5,870,433	2/9/99	Huber et al.			
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	MM	6,201,831	3/13/01	Agazzi et al.			

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EXAMINER	INITIAL	DOCUMENT NO.	DATE	COUNTRY	CLASS/SUBCLASS	TRANSLATION	YES	NO

## OTHER DOCUMENTS

EXAMINER	INITIAL	REF NO.	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	PH	1.	Keshab K. Parhi, "Pipelining in Algorithms with Quantizer Loops," IEEE Transactions on Circuits and Systems, Vol. 38. No. 7, 745-754 (July 1991)
	PH	2.	Bednarz et al., "Design, Performance, and Extensions of the RAM-DFE Architecture," IEEE Transactions on Magnetics, Vol. 31, No. 2, 1196-1201 (March 1995)

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*phuong phu*

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